In the claims:

1-23 (Cancelled)

24 (Currently amended) A Signal processing system for a wireless communications system, said signal processing system comprising:

a baseband receiver having one or more control inputs, quadrature outputs and a status output;

a transmit modulator having a quadrature input, one or more control inputs, and a status output;

a baseband receive processor having one or more control outputs, a multiplexer control, and a quadrature input;

a baseband transmit processor having a quadrature output, a sample output, and a transmit enable output;

a first multiplexer having an output which selects between one of:

said baseband receive processor control outputs or one of said baseband transmit processor quadrature outputs in response to said transmit enable, said first multiplexer output coupled to a first digital to analog converter (DAC), and delivering said first DAC output to one of said transmit modulator quadrature inputs and also to one of said baseband receiver control inputs;

a sample and hold having an input coupled to said first DAC output and an output coupled to one of said transmit

modulator control signals, said sample and hold controlled by said baseband transmit processor said sample output;

a second multiplexer having an output, said second multiplexer output coupled to one of:

other said baseband receive processor control output or the other of said baseband transmit processor quadrature output in response to said transmit select, said second multiplexer output coupled to a second digital to analog converter (DAC) and delivering said second DAC output to the other of said transmit modulator quadrature inputs and also to the other of said baseband receiver control inputs;

a third multiplexer having an output, said third multiplexer output coupled to either of:

one of said baseband receiver quadrature outputs or said baseband receiver status signal in response to said baseband receiver processor said multiplexer control, said third multiplexer output coupled to a first analog to digital converter, the output of said analog to digital converted coupled to said baseband receive processor status signal and also to one of said baseband receiver quadrature inputs;

a fourth multiplexer having an output, said fourth multiplexer output coupled to one of:

~~the other said baseband receiver quadrature output or said transmit modulator status signal, said fourth multiplexer output coupled to one o?~~

the other said baseband receiver quadrature output or said transmit modulator status signal, said fourth multiplexer selection controlled by said baseband transmit processor said transmit enable, said fourth multiplexer output coupled to a second analog to digital converter (ADC), the output of said second ADC coupled to the other said receive processor quadrature input and said baseband transmit processor status signal.

25 (Original) The signal processing system of claim 24 where said first multiplexer couples one of said baseband receive processor control signals to said first DAC when said transmit enable is not active.

26 (Original) The signal processing system of claim 25 where said baseband receive processor control signal is a gain control signal.

27 (Original) The signal processing system of claim 24 where said first multiplexer couples one of said baseband transmit processor quadrature signals to said first DAC when said transmit enable is active.

28 (Original) The signal processing system of claim 24 where second multiplexer couples one of said baseband

receive processor control signals to said second DAC when said transmit enable is not active.

29 (Original) The signal processing system of claim 28 where said baseband receive processor control signal is a gain control signal.

30 (Original) The signal processing system of claim 24 where said second multiplexer couples one of said baseband transmit processor quadrature signals to said DAC when said transmit enable is active.

31 (Original) The signal processing system of claim 24 where said third multiplexer couples said baseband receiver status signal to said ADC when said receive processor said multiplexer control is not active.

32 (Original) The signal processing system of claim 31 where said baseband receiver status signal is receive signal strength indication.

33 (Original) The signal processing system of claim 24 where said third multiplexer couples one of said baseband receiver quadrature outputs to said first ADC when said receiver processor said multiplexer control is active.

34 (Original) The signal processing system of claim 24 where a transmit gain value is placed on one of said baseband transmit processor quadrature outputs and said sample output is active.

35 (Original) The signal processing system of claim 24 where at least one of said baseband receive processor or said baseband transmit processor is a digital circuit.

36 (Original) The signal processing system of claim 35 where said digital circuit is an integrated circuit

37 (Original) The signal processing system of claim 35 where said digital circuit is a field programmable gate array (FPGA).

38-41 (Cancelled)

42 (Original) The signal processing system of claim 24 where said third multiplexer includes a test input which is coupled to said first DAC or to said DAC.

43 (Original) The signal processing system of claim 24 where said fourth multiplexer includes a test input which is coupled to said first DAC or to said DAC.

44 (Cancelled)